SURFACE VOLTAGE SUSTAINING STRUCTURE FOR SEMICONDUCTOR DEVICES

TECHNICAL FIELD

This invention relates to a semiconductor high-voltage and high power device, and more particularly to a surface voltage sustaining structure for semiconductor devices.

BACKGROUND OF THE INVENTION

It is well known that the breakdown voltage of a planar n^+-p^- (or p^+-n^-) junction is normally restricted by the surface breakdown. This phenomenon is explained by FIG. 1, a cross-sectional region of a planar n^+-p^- (or p^+-n^-)-junction, as follows.

In FIG. 1, 1 refers to a p^- (or n^-)-substrate, 2 refers to an n^+ (or p^+)-region. Under a reverse voltage, the field along a middle line of the structure is vertical with a maximum value at an n^+-p^- (or p^+-n^-) metallurgical junction with its integral along the said line equal to the reverse voltage, whereas the field along the surface has almost only lateral component with its integral along the surface also equal to the reverse voltage. Owing to the curvature effect, the field along the surface is very uneven and has a very high value near the n^+ (or p^+)-structure. This high field normally causes the breakdown voltage of avalanche impact ionization much lower than that of an one-sided parallel plane junction with the same substrate.

In order to enhance the surface breakdown voltage of the planar junction, there are a number of techniques available, called planar junction termination techniques (JTT's). For references of planar JTT's see: [1] B. J. Baliga, IEE proc., vol. 129, Pt. I, No. 5, pp. 173–179 (1982). Among the planar JTT's, there are only three techniques that can make the breakdown voltage reach 90% of that of a one-sided parallel plane junction with the same substrate: junction termination extension (JTE), variational lateral doping (VLD) and resistivity field plate (RFP). With the JTE technique, one can not obtain a maximum breakdown voltage with the smallest distance on the surface. With the conventional VLD technique, deep diffusion of the junctions must be used, which is not compatible with modern sub-micron technology. With the RFP technique, additional complicated technology is needed to fabricate a resistive film. Moreover, with any of the said three techniques, the surface voltage sustaining structure can not be simultaneously a drift region with low on-resistance for the lateral devices.

In order to improve the breakdown voltage as well as to reduce the on-resistance of the lateral MOST, there are two techniques available namely, the offset-gate technique and the reduced surface field (RESURF) technique. For references of these two techniques see: [2] S. Ochi, et al., IEEE Trans. Electron Devices, vol. ED-27, p. 399 (1980); [3] E. J. Wildi, et al., IEDM Digest p. 268 (1982). However, both of these two techniques normally need a particular ion-implantation process, and they yield lower on-resistance (for MOST's) or lower base-resistance (for vertical bipolar transistors) while higher breakdown voltage is obtained.

SUMMARY OF THE INVENTION

The object of the present invention is to provide a new surface voltage sustaining structure. By using the surface voltage sustaining structure of this invention, the highest breakdown voltage with the smallest surface distance can be obtained in a semiconductor substrate with a certain

resistivity, and lower on-resistance (for MOSTs') or lower base-resistance (for vertical bipolar transistors) can be obtained. The structure of the present invention accommodates considerable flexibility for making the high voltage devices compatible with the modern sub-micron technology. Based upon such flexibility, high voltage integrated circuits (HVIC's) and power integrated circuits (PIC's) with higher performances and lower costs can also be implemented in BiCMOS and CMOS.

This invention is conceived from a theory of optimum variational lateral doping proposed by the inventor, see reference [4] X. B. Chen, et al., Solid-State Electronics, vol. 35, pp. 1365–1370 (1992). However, different structures to approach such optimum variational lateral doping and their application to different devices are provided in this invention.

The object of the present invention is realized by a surface voltage sustaining structure for a semiconductor device of the present invention, the semiconductor device is based on a heavily doped region of a second conductivity type on the top of a lightly doped substrate of a first conductivity type. The surface voltage sustaining structure of the present invention is located around said heavily doped region, and has an average doping density of the second conductivity type decreasing from a value about $N_B W_{pp}$ gradually or stepwisely with the increasing of the distance to said heavily doped region of a second conductivity type, under the condition that said structure is totally depleted under a reverse voltage close to the breakdown voltage applied to said heavily doped region of a second conductivity type and the substrate, where N_B is the doping concentration of the substrate, W_{pp} is the depletion width of an abrupt parallel plane junction made by the substrate under its breakdown voltage, and the average doping density of the second conductivity type refers to the average number of the effective ionized impurity atoms of the second conductivity type in a surface area, which has a lateral dimension much smaller than W_{pp} but larger than the thickness of the surface region.

The present invention also provides a surface voltage sustaining structure, wherein the average doping density of the second conductivity type in the surface voltage sustaining structure is formed by a local compensation of the impurity atoms of the first conductivity type of at least one region of the first conductivity type in the surface voltage sustaining structure to the impurity atoms of the second conductivity type of at least one region of the second conductivity type in the surgace voltage sustaining structure, where the bottom of the surface voltage sustaining structure is a region of the second conductivity type, and the average doping density of the second conductivity type refers to the average number of ionized impurities of the second conductivity type in the region (s) of the second conductivity type deducted by the average number of ionized impurities of the first conductivity type in the region(s) of the first conductivity type in the surface area.

The present invention still provides a surface voltage sustaining structure, wherein a region with uniform doping density of the second conductivity type is used and the region of the first conductivity type for compensation on the top has several structures as follows:

a) multiple continuous zones with impurity density of the first conductivity type increased zone by zone in accordance with the distance to the said heavily doped region of a second conductivity type;

b) at least one zone in the region of the first conductivity type is replaced by a plurality of separate small zones of the first conductivity type;